Low Power, 3-channel 6dB gain Video buffer for HD-Video

Features

- 3-HDTV Video Filter Support Y'Pb'Pr',R'G'B' or VGA/SVGA/XGA
- Ultra wide bandwidth: 220MHz
- Ultra low Propagation Delay:1.8ns(100KHz-60MHz)
- Slew rate:1,000V/us
- Very Low Quiescent Current: 11 mA/channel (at 3.3V, Typical)
- 6dB Gain(2V/V), Rail to Rail Output
- AC- or DC-Coupled Output Driving Dual Video Loads (75Ω)
- Wide Power Supply: +3.0V to +5.5V Single Supply
- Robust ESD Protection:
  - Robust 8kV – HBM and 2kV – CDM ESD Rating
- Green Product, SOIC-8 Package

Applications

- Set-Top Box and VOD Video buffer
- PVR、DVD Player Video Buffer
- Video Buffer for Portable or USB-Powered Video Devices
- HDTV
- Projector Video Signal Amplification

Description

TPF153 is low power consumption; single power supply (3.3V/5.5V), three channel video buffers, and it have 6dB gain with 220MHz 3dB bandwidth, which is suitable for Y'Pb'Pr', R'G'B', VGA/SVGA/XGA

TPF153 is perfect to support HD video with very low power consumption; its high dynamic range can meet the most challenge HD system requirement.

As part of the TPF153 flexibility, the input can be configured for ac- or dc-coupled inputs. The 84-mV output level shift allows for a full sync dynamic range at the output with 0-V input. The ac-coupled modes include a transparent sync-tip clamp option for Y', and G'B'R' signals. AC- coupled biasing for C'/P'B/P'R channels can easily be achieved by adding an external resistor to VS+.

The TPF153 rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive two lines, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 34.5-mA total quiescent current at 3.3 V makes it an excellent choice for power-sensitive video applications.

TPF153 is available in SOIC-8 package. Its operation temperature range is from −40°C to +85°C.

Related Resources

AN-1201: Application notes of TPF1

Function Block

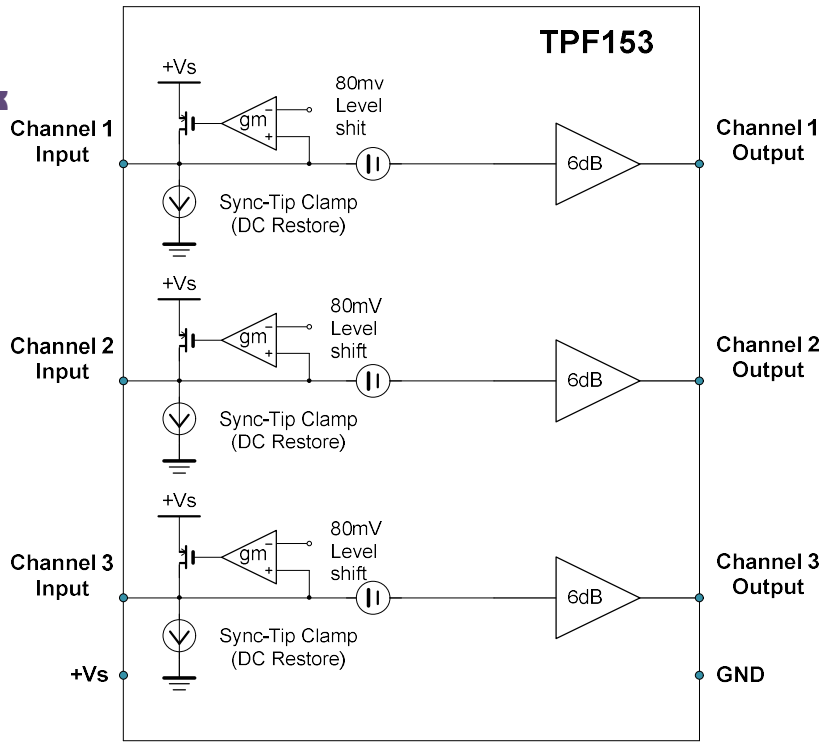


Figure 1

Order Information

Order Number	Operating Temperature Range	Package	Package Options	Transport Media, Quantity
TPF153-SR	-40 to 85°C	SOIC-8	MSL-3	Tape and Reel, 4000

Pin configuration (Top View)

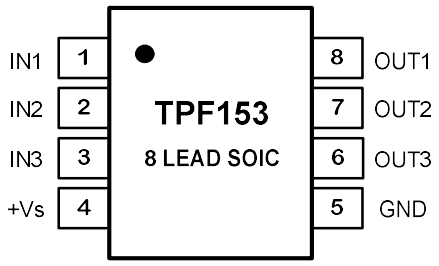


Figure 2.

Pin Number	Pin Name	Function
1	IN1	First Input
2	IN2	Second input
3	IN3	Third input
4	$+V_S$	Positive power supply
5	GND	Ground
6	OUT3	Third output
7	OUT2	Second output
8	OUT1	First output

Absolute Maximum Ratings*

Parameters		Value	Units
Power Supply, V_{DD} to GND		6.0	V
PD	Power Dissipation，TA = 25°C，8-Lead SOIC	800(1)	PD
V_{IN}	Input Voltage	V_{DD} + 0.3V to GND - 0.3V	
I_O	Output Current	65	I_O
T_J	Maximum Junction Temperature	150	T_J
T_A	Operating Temperature Range	–45 to 85	T_A
T_{STG}	Storage Temperature Range	–65 to 150	T_{STG}
TL	Lead Temperature (Soldering 10 sec)	300	TL
θ_{JA}	8-Lead SOIC Thermal Resistance	130(2)	θ_{JA}

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Electrical Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Electrical Specifications						
V_{DD}	Supply Voltage Range		3.0		5.5	V
I_{CC}	Quiescent current (I_Q) (1)	V_{DD} = 3.3V, V_{IN} = 500mV, no load		33	41	mA
		V_{DD} = 5.0V, V_{IN} = 500mV, no load		43.1	53.2	mA
V_{OLS}	Output Level Shift Voltage	V_{IN} = 0V, no load, input referred	54	80	124	mV
$I_{CLAMP-CHG}$	Clamp Charge Current	V_{IN} = V_{CLAMP} - 100mV	-1.5	-1.7		mA
$I_{CLAMP-DCHG}$	Clamp Discharge Current	V_{IN} = 500mV	1.1	4.0	7.1	μA
V_{CLAMP}	Input Voltage Clamp	I_{IN} = -1mA	-40	0	+40	mV
AV	Voltage Gain	V_{IN}=0.5V,1V or 2V R_L=150Ω to GND	5.91	6.01	6.03	dB
PSRR	Power Supply Rejection Ratio	ΔV_{DD} = 3.3V to 3.6V		64		dB
		ΔV_{DD} = 5.0V to 5.5V, 50Hz, V_{IN}=0.7V		76		dB
V_{OH}	Output Voltage High Swing	V_{IN} = 3V, R_L =75Ω to GND (dual load)		3.18		V
V_{OL}	Output Voltage Low Swing	V_{IN} = -0.3V, R_L =75Ω		0.05		V
I_{SC}	Short-circuit current	V_{IN} =2V, output to GND through 10Ω	65			mA
		V_{IN}=100mV, output short to V_{DD}	65			mA
AC Electrical Specifications						
f_{-1dB}	-1dB Bandwidth	R_L=150Ω	144	167		MHz
f_{-3dB}	-3dB Bandwidth	R_L=150Ω	192	220		MHz
SR	Slew Rate	2V output step, 80% to 20%		1,000		V/μs
dG	Differential Gain	Video input range 1V		0.4	0.7	%
dP	Differential Phase	Video input range 1V		0.3	0.5	°
THD	Total Harmonic Distortion	f=22MHz, V_{OUT}=1.4V_{PP}		0.2		%
D/DT	Group Delay Variation	f = 100kHz to 60MHz		0.5		ns
t_{PD}	Propagation Delay	Maximum delay from input to output: (100kHz to 60MHz)		1.8	2.2	ns
X_{TALK}	Channel Crosstalk	f = 1MHz, V_{OUT}=1.4V_{PP}	-68	-74		dB
SNR	Signal-to-Noise Ration	f= 100kHz to 60MHz	70	73		dB
R_{OUT_AC}	Output Impedance	f = 10MHz		0.5		Ω

Note:

(1). 100% tested at T_A=25°C.

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

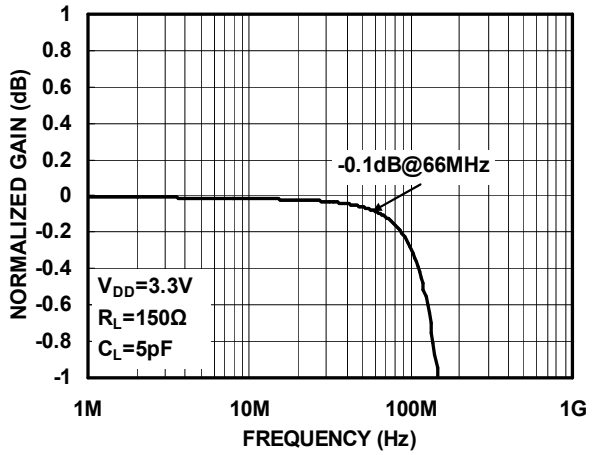


Figure3. Small-Scale Frequency Response

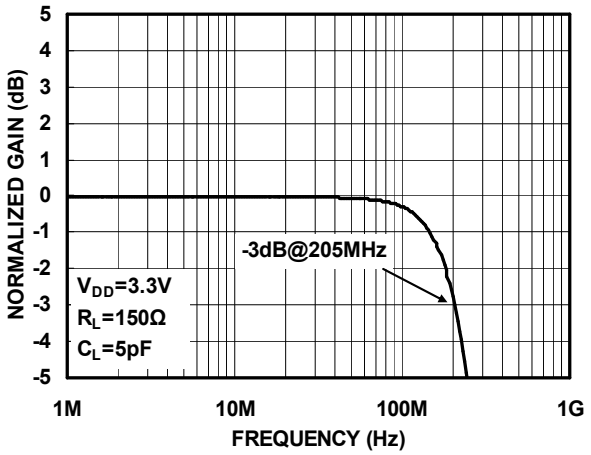


Figure4. Large-Scale Frequency Response

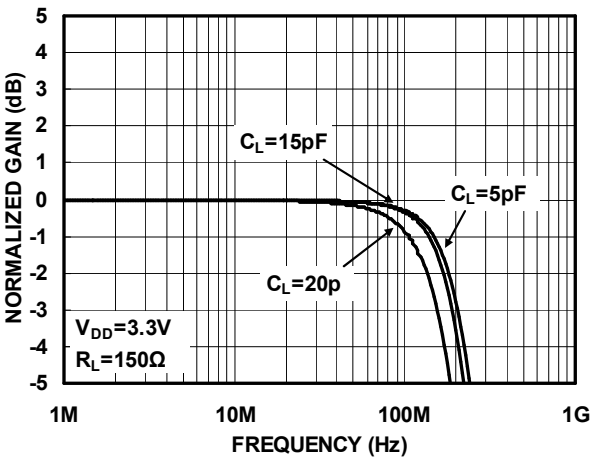


Figure5. Gain Vs. Frequency With C_{LOAD}

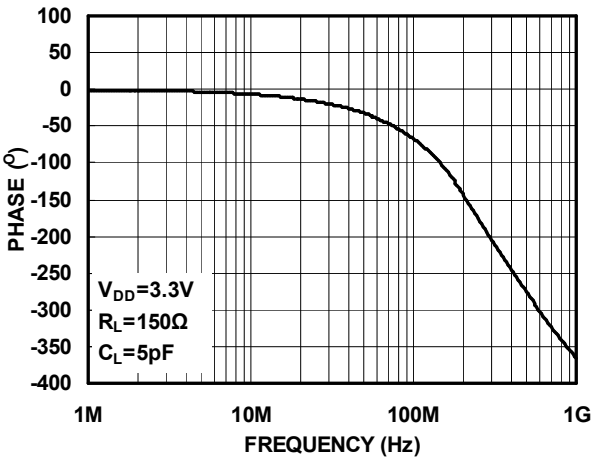


Figure6. phase Vs. Frequency

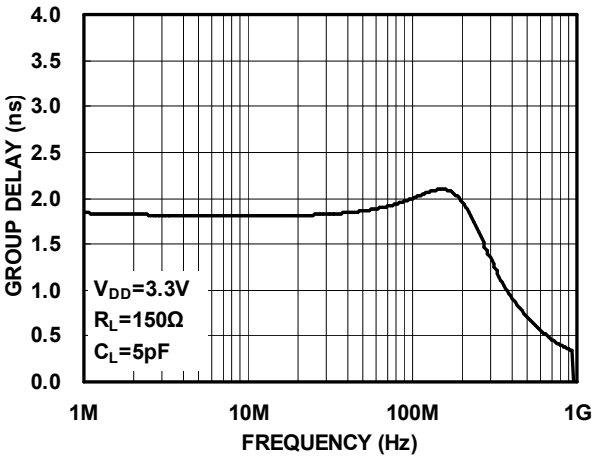


Figure7. Group Delay vs Frequency

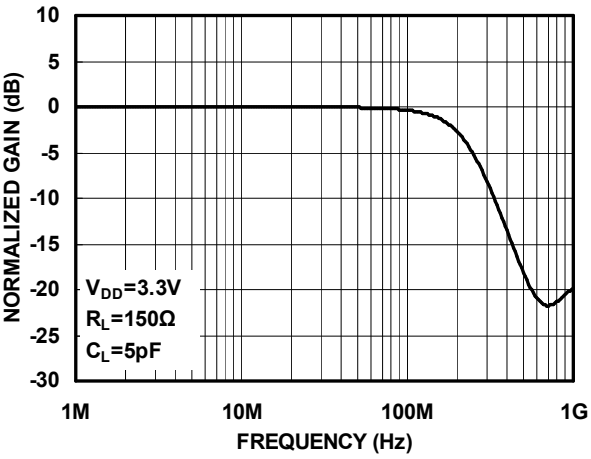


Figure8. Stop Band Attenuation

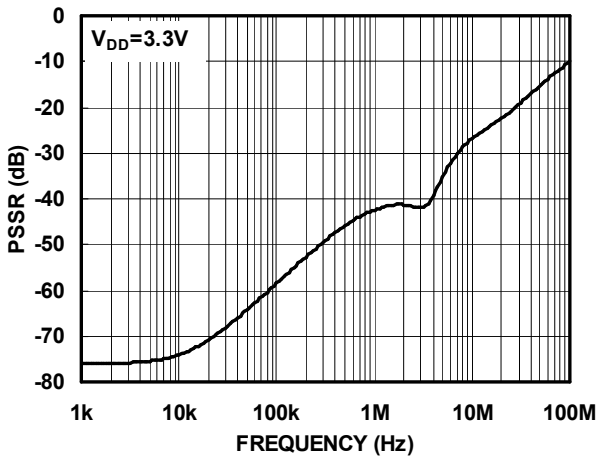


Figure9. PSRR Vs. Frequency

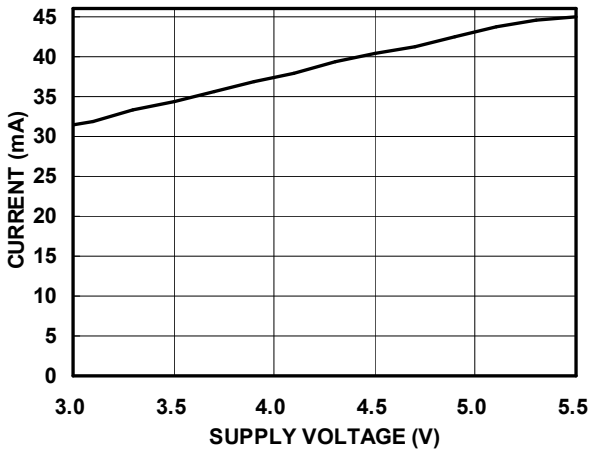


Figure10. Current Vs. Supply Voltage

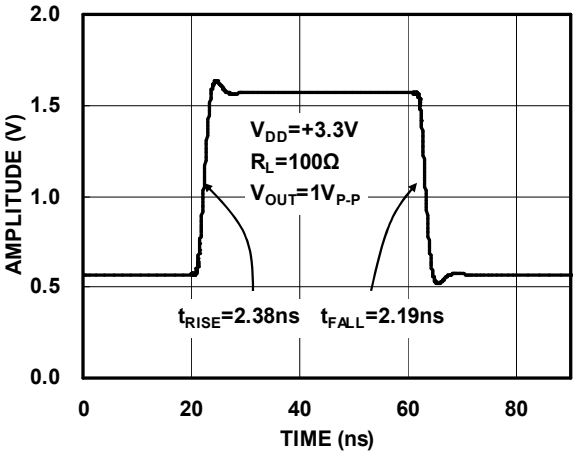


Figure11. Large-Signal Pulse Response Vs. Time

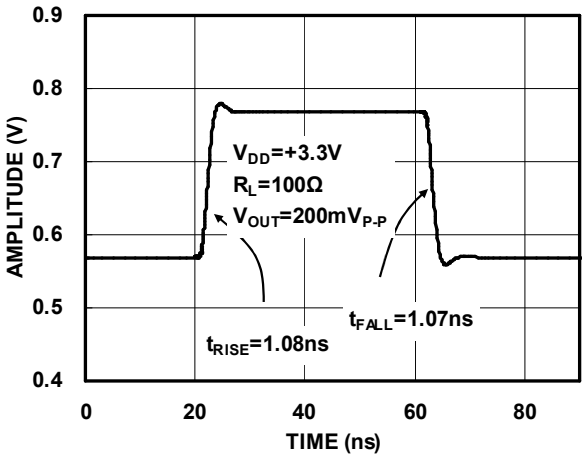


Figure12. Small-Signal Pulse Response Vs. Time

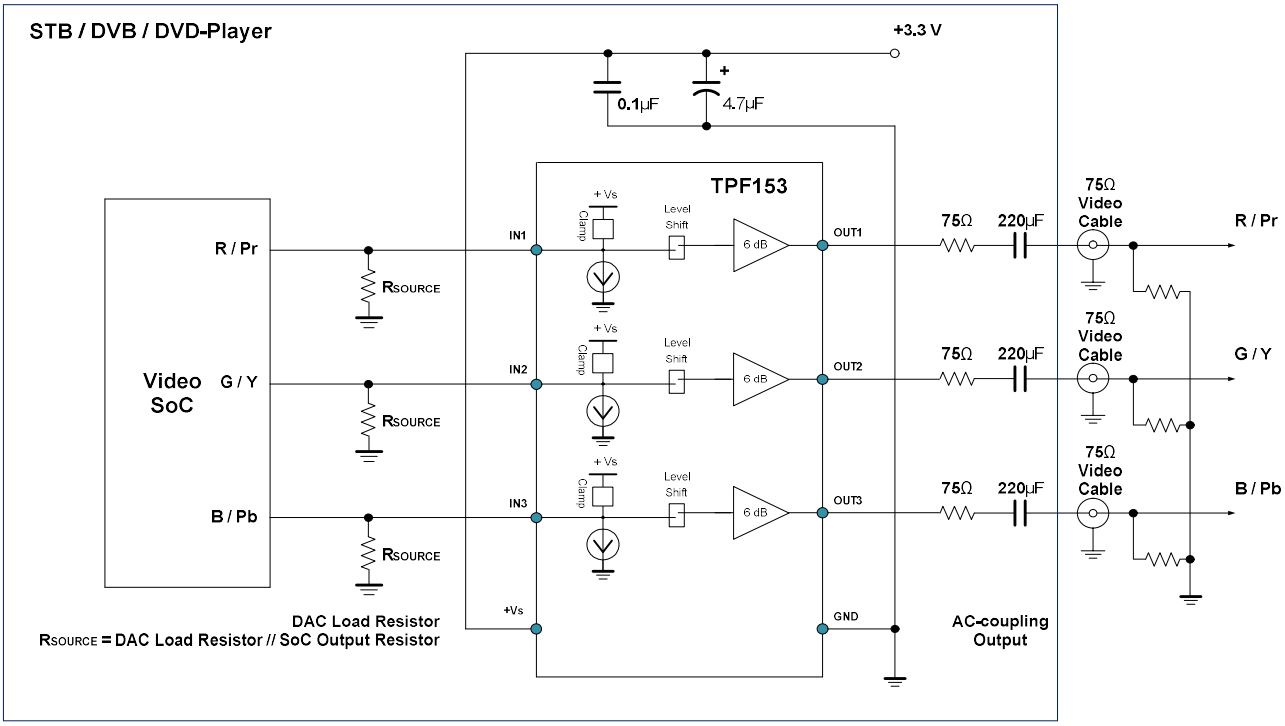


Figure13. Reference Design

Application Information

The TPF153 is a single power supply, rail to rail, three channel HD video buffer, it can support Y'Pb'Pr'-1080p/1080i/720p、R'G'B' or VGA /SVGA /XGA HD video signal application, it integrate internal sync clamp, typical 3dB BW 220MHz, slew rate 1,000V/us, which is very good for low power consumption and wide band video amplification application.

Internal Sync Clamp

The typical embedded video DAC operates from a ground referenced single supply. This becomes an issue because the lower level of the sync pulse output may be at a 0V reference level to some positive level. The problem is presenting a 0V input to most single supply driven amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degrading the video image. A larger positive reference may offset the input above its positive range.

The TPF153 features an internal sync clamp and offset function to level shift the entire video signal to the best level before it reaches the input of the amplifier stage. These features are also helpful to avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram of the TPF153 in Figure-1. The AC coupled video sync signal is pulled negative by a current source at the input of the comparator amplifier. When the sync tip goes below the comparator threshold the output comparator is driven negative, The PMOS device turns on clamping sync tip to near ground level. The network triggers on the sync tip of video signal.

Droop Voltage and DC Restoration

Selection of the input AC-coupling capacitance is based on the system requirements. A typical sync tip width of a 64μs NTSC line is 4μs during which clamp circuit restores its DC level. In the remaining 60μs period, the voltage droops because of a small constant 2.0μA sinking current. If the AC-coupling capacitance is 0.1μF, the maximum droop voltage is about 1mV which is restored by the clamp circuit. The maximum pull-up current of the clamp circuit is 1.7mA. For a 4μs sync tip width and 0.1μF capacitor, the maximum restoration voltage is about 80mV.

The line droop voltage will increase if a smaller AC-coupling capacitance is used. For the same reason, if larger capacitance is used the line droop voltage will decrease.

Output Couple

TPF153 output could support both “AC Couple” and “DC Couple”, if use “AC Couple”, this capacitor is typically between 220-μF and 1000-μF, although 470-μF is common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document.

The TPF153 internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, thereby saving board space and additional expense for capacitors. This makes the TPF153 extremely attractive for portable video applications. Additionally, this solution completely eliminates the issue of field tilt in the lower frequency. The trade off is greater demand of supply current. Typical load current for AC coupled is around 1mA, compared to typical 6.6mA used when DC coupling.

Output Drive Capability and Power Dissipation

With the high output drive capability of the TPF153, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area. The maximum power dissipation allowed in a package is determined according to Equation:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where：

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature
Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or: for sourcing:

$$PD_{MAX} = V_s \times I_{SMAX} + (V_s - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

Where:
V_S = Supply voltage
I_{SMAX} = Maximum quiescent supply current
V_{OUT} = Maximum output voltage of the application
R_{LOAD} = Load resistance tied to ground

By setting the two PDMAX equations equal to each other, we can solve the output current and RLOAD to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

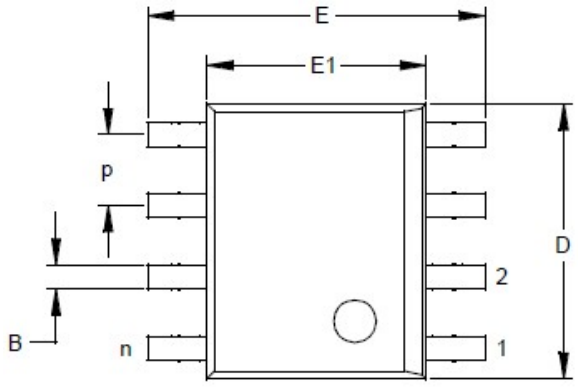
As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor from VS+ to GND will suffice.

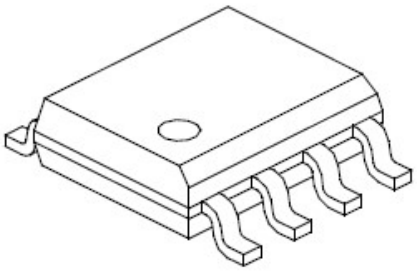
VIDEO FILTER DRIVER SELECTION GUIDE

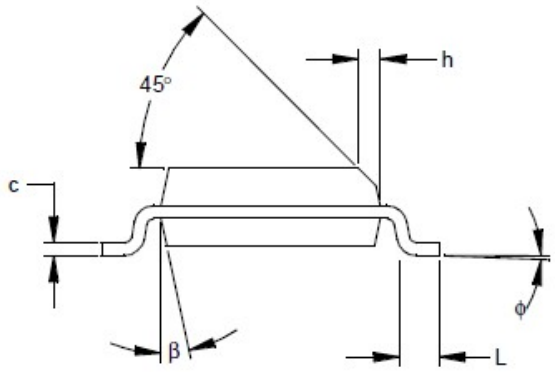
P/N	Product Description	Channel	-3dB Bandwidth	Package
TPF110 /TPF110L	Low power, enable function and SAG correction, 1 channel 6th order 9MHz	1-SD	9MHz	SC70-5 SOT23-6
TPF113	Low power 3 channel, 6th-order 9MHz SD video filter	3-SD	9MHz	SO-8
TPF114	Low power 4 channel, 6th-order 9MHz SD video filter	4-SD	9MHz	MSOP-10 TSSOP-14
TPF116	Low power 4 channel, 6th-order 9MHz SD video filter for CVBS, SVIDEO	6-SD	9MHz	TSSOP-14
TPF123	3 channel 6th-order 13.5MHz, 960H/720H-CVBS video filter or Y'Pb'Pr 480P/576P video filter	3-ED	13.5MHz	SO-8
TPF133	Low power 3 channel, 6th-order 36MHz HD video filter	3-HD	36MHz	SO-8
TPF134	Low power 3 channel, 6th-order 36MHz HD video filter and 1 channel SD video filter	1-SD& 3-SD	9MHz 36MHz	MSOP-10 TSSOP-14
TPF136	Low power 3 channel, 6th-order 36MHz HD video filter and 3 channel SD video filter	3-SD& 3-HD	9MHz 36MHz	TSSOP-20
TPF143	Low power 3 channel, 6th-order 72MHz Full HD video filter	3-FHD	72MHz	SO-8
TPF144	Low power 3 channel, 6th-order 72MHz Full HD video filter and 1	1-SD& 3-FHD	9MHz 72MHz	MSOP-10 TSSOP-14

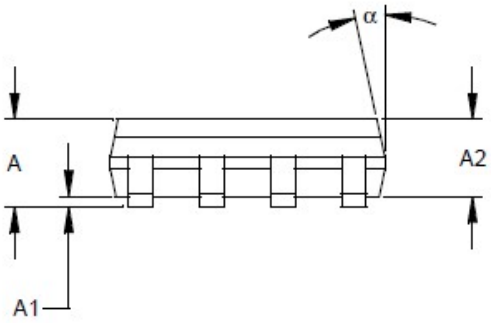
	channel SD video filter			
TPF146	Low power 3 channel, 6th-order 72MHz Full HD video filter and3 channel SD video filter	3-SD& 3-FHD	9MHz 72MHz	TSSOP-20
TPF153	Low power 3 channel, 6th-order 220MHz Full HD video filter	3-CH	220MHz	SO-8

Package Outline Dimensions









Symbol	inch			mm		
	min	Typical	maxim	min	Typical	maxim
n		8			8	
p		.050			1.27	
A	.053	.061	.069	1.35	1.55	1.75
A2	.052	.056	.061	1.32	1.42	1.55
A1	.004	.007	.010	0.10	0.18	0.25
E	.228	.237	.244	5.79	6.02	6.20
E1	.146	.154	.157	3.71	3.91	3.99
D	.189	.193	.197	4.80	4.90	5.00
h	.010	.015	.020	0.25	0.38	0.51
L	.019	.025	.030	0.48	0.62	0.76
Φ	0	4	8	0	4	8
c	.008	.009	.010	0.20	0.23	0.25
B	.013	.017	.020	0.33	0.42	0.51
α	0	12	15	0	12	15
β	0	12	15	0	12	15

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